## AMENDMENTS TO THE DRAWINGS

Fig. 16 has been amended to illustrate a primary anchor and a secondary anchor.

Attachment: 1 Annotated Sheet
1 Replacement Sheet

## REMARKS

In the present Amendment, Fig. 16 has been amended to illustrate a primary anchor and a secondary anchor. This amendment is supported by the specification, for example, at page 33, lines 13-16. Claims 24, 25, 32, 37, 40-42, 52 and 57 have been amended. The amendment to claim 24 is supported by the specification, for example, by Fig. 12(c), and at page 39, line 28 to page 43, line 30. The amendment to claim 32 is supported by the specification, for example, by Fig. 23 and at page 99, lines 3 to 10. The amendment to claim 37 is supported by the specification, for example, Fig. 33 (F) (5028), and at page 68, lines 32 to 35. The amendment to claim 40 is supported by the specification, for example, Fig. 44. The amendment to claim 41 is supported by the specification, for example, by Figs. 44 to 46. The amendment to claim 52 is supported by the specification, for example, page 49, lines 16 to 26. Claims 25, 37, 42 and 57 have been amended for clarity.

In addition, claims 58-63 have been added. Claims 58 and 60 are supported by the specification, for example, at page 113, lines 20 to 23. Claim 59 is supported by the specification, for example, by Fig. 33(H) and at page 117, lines 16 to 18. Claim 61 is supported by the specification, for example, by Fig. 39(E) and at page 124, lines 1 to 3. Claim 62 is supported, for example, by Fig. 44. Claim 63 is supported by the specification, for example, at page 37, lines 28 to 29.

Claim 22 has been canceled. Claims 1-8, 14-21, 27-31, 33-36, 39 and 47 have previously been canceled.

No new matter has been added and entry of the Amendment is respectfully submitted to be proper. Upon entry of the Amendment, claims 9 to 13, 23 to 26, 32, 37, 38, 40 to 46 and 48 to 63 will be all the claims pending in the application.

Applicants note with appreciation that claims 9 to 13 and 48 to 51 are allowed.

In the Office Action, the drawings are objected to. Claims 24 and 57 were rejected under 35 U.S.C. § 102(b) as allegedly being anticipated by Furui (U.S. Pat. No. 5,258,094). Moreover, claims 32, 37, 38, 40-45 and 57 were rejected under 35 U.S.C. § 102(e) as allegedly being anticipated by Chong (U.S. Pat. No. 5,699,613). Further, claims 22, 23 and 52 were rejected under 35 U.S.C. § 103(a) as allegedly being unpatentable over Greschner (U.S. Pat. No. 4,642,163) in view of Kosaka (U.S. Pat. No. 5,200,271). Furthermore, claims 25, 26 and 56 were rejected under 35 U.S.C. § 103(a) as allegedly being unpatentable over Greschner in view of Kosaka and further in view of Suzuki (U.S. Pat. No. 5,021,296[1]). Lastly, claim 54 was rejected under 35 U.S.C. § 103(a) as allegedly being unpatentable over Furui in view of Greschner.

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[1] Suzuki is identified to be U.S. Pat. No. 5,589,255. However, Applicants believe that the correct Pat. No. is 5,021,296, which was cited on the Form PTO-892 attached to the Office Action dated August 10, 2004.

## I. Response to Drawing Objection

It was asserted in the Office Action that the limitation "wherein said roughened surface comprises a primary anchor and a secondary anchor" is not shown in the drawings.

In response, Applicants have amended Fig. 16 to illustrate a primary anchor and a secondary anchor. The amendment is supported by the disclosure in the specification, e.g., at page 33, lines 13-16. Accordingly, the Examiner is respectfully requested to reconsider and withdraw the objection.

## II. Response to Rejection of Claims 24 and 57 under 35 U.S.C. § 102(b) over Furui

Applicants respectfully submit that present claims 24 and 57 are novel and patentable over Furui for at least the following reasons.

Claim 57 depends from claim 32 and thus contains all the limitations of claim 32. Claim 32 is not included in the rejection. Accordingly, Applicants respectfully submit that claim 57 should not be included in the rejection. However, Applicants note that claim 55 depends from claim 24 and will address below claim 55 in addition to claim 24.

In the printed circuit board according to the present invention (claim 24), peeling of the plated film can be prevented, and a sufficiently thick plated metal film can be formed on the hole bottoms, as described at page 37, lines 7 to 12 of the present specification, even when the openings for via holes are fine. With respect to the electroless plated film in the via hole, for

example, the area of contact with the lower-layer conductor circuit increases considerably due to the roughened surface of the lower-layer conductor circuit. As a result, the adhesive strength increases. Further, the electroless plated film bites into the irregularities of the roughened surface of the lower-layer conductor circuit.

The above-mentioned plated film has several interfaces: the interface between the lower-layer conductor circuit and the interlayer resin insulating layer; the interface between the interlayer resin insulating layer and the upper-layer conductor circuit; and the interface between the lower-layer conductor circuit and the upper-layer conductor circuit.

According to the present invention, the lower-layer conductor circuit and the interlayer resin insulating layer on the lower-layer conductor circuit ensure adhesion by the roughened surface of the lower-layer conductor circuit. The interlayer resin insulating layer and the upper-layer conductor circuit ensure adhesion by the roughened surface of the interlayer resin insulated layer.

The interface between the lower-layer conductor circuit and the upper-layer conductor circuit exists in the via hole, namely, the surface of the lower-layer conductor circuit 2004a in Fig. 13(a)) and the surface of the electroless plated film (2012 in Fig. 13(a)). As described at page 4, line 27 to 28 of the specification, an electroless plated film has a compressive stress (an expanding force) and tends to peel off. Further, the thicker the electroless plated film is, the greater the compressive stress accumulates. According to the present invention (claim 24), the

electroless plated film formed on the bottom of the via hole has a thickness equal to 50% to 100% of the thickness of the electroless plated film formed on the interlayer resin insulating layer so as to reduce the compressive stress. Further, because of the roughened surface of the lower-layer conductor circuit, the area of contact between the electroless plated film and the lower-layer conductor circuit is increased. Accordingly, even at a fine via hole where a peeling of the electroless plated film tends to occur, the peeling at the interface is suppressed.

Concerning Furui, the Examiner considers that the multilayered board 14, the conductive layer 63, the insulating resin layer 9, and the conductive layer 64, respectively, correspond to the substrate board (2001 in Fig. 13(a)), the lower-layer conductor circuit (2004 in Fig. 13(a)), the interlayer resin insulating layer (2002 in Fig. 13(a)), and the upper-layer conductor circuit (2012 and 2013 in Fig. 13 (a)) of the present invention. However, in Furui, the insulating resin layer 9 is not disposed between the conductive layer 63 and the conductive layer 64. That is, the insulating resin layer 9 of Furui does not correspond to the interlayer resin insulating layer of the present invention.

Applicants now assume that the prepreg layer 52 of Furui, instead of the insulating resin layer 9, may correspond to the interlayer resin insulating layer of the present invention.

While the lower-layer conductor circuit of the present invention (2004) has a roughened surface on a side which contacts with the interlayer resin insulating layer (2002), the conductive layer 63 of Furui does not have a roughened surface on a side which contacts with the prepreg

layer 52. Further, while the present invention teaches that the electroless plated film formed on the bottom of the via hole has a thickness equal to 50% to 100% of the thickness of the electroless plated film formed on the interlayer resin insulating layer, Furui is silent about the ratio of the thickness of the electroless plated film in the photoviahole 42 and that of the electroless plated film on the prepreg layer 52. Moreover, while the lower-layer conductor circuit of the present invention connects with the electroless plated film formed on the bottom of the via hole through the roughened surface of the lower-layer conductor circuit, the conductive layer 63 of Furui does not connect with the electroless plated film of the conductive layer 64 in the photoviahole 42.

In view of the above, it is seen that the multilayered board of Furui is different from the presently claimed printed circuit board. That is, Furui does not teach or anticipate the constitution of the present invention.

In addition, Furui does not teach or suggest the effects of the present invention. As mentioned above, according to the present invention, the adhesion between the lower-layer conductor circuit and the interlayer resin insulating layer, between the interlayer resin insulating layer and the upper-layer conductor circuit, and between the lower-layer conductor circuit and the upper-layer conductor circuit are ensured by the roughened surfaces. This effect is especially significant when the diameter of the via hole is as small as, for example, 80 μm or less (claim 55).

In view of the foregoing, Applicants respectfully submit that claims 24 and 55 are neither anticipated by, nor obvious over Furui, and thus the § 102 rejection should be withdrawn.

## III. Response to § 102(e) Rejection of Claims 32, 37, 38, 40 to 46 and 57 over Chong

Applicants respectfully submit that present claims 32, 37, 38, 40 to 46 and 57 are novel and patentable over Chong for at least the following reasons.

### a. Chong

Chong discloses a multiple layer circuit board structure. The multiple layer circuit board comprises the base laminate 1, conductive patterns 36 on the base laminate 1 having on both sides the conductive patterns 12, the dielectric material 23 on each of the conductive patterns 12, and the plating 31 and the conductive polymer 32 constituting the vias 24 and 26 to 29. Vias 26 and 29 are formed on the through hole 16 which extends through the base laminate 1.

### b. Present Claim 32

According to the presently claimed invention as defined in claim 32, especially with the conductor circuits having the thickness not greater by more than 10 μm than the thickness of the conductor layer on the interlayer resin insulating layer, the multilayer printed circuit board can attain an elaborate circuit, an impedance alignment between the conductor circuit on the core board and the conductor layer on the interlayer resin insulating layer (see page 55, lines 4 to 9 of the present specification), and a heat cycle resistance.

Present claim 32 recites that the thickness of each of the conductor circuits is not greater by more than 10 μm than the thickness of the conductor layer on said interlayer resin insulating layer in the range of 10 to 30 μm. Such thin conductor circuits can realize elaborate circuits. Further, since the thickness difference between the conductor circuits and the conductor layer is small, the impedance alignment can be attained easily and a high-frequency characteristic of the multilayer printed circuit board can be improved. Moreover, the small thickness difference suppresses cracks in the interlayer resin insulating layer since stress does not accumulate in the corners of the conductor circuits and the conductor layer.

It was asserted that Chong teaches the thickness difference between the conductor circuits (analogous to conductive patterns 36) and the conductor layer (analogous to the plating 31). However, Chong is silent about the thickness difference. Further, Chong does not teach about the effects achieved by adjusting the thickness difference. Accordingly, a skilled person would not be motivated by Chong to attain the present invention.

In view of the foregoing, Applicants respectfully submit that present claim 32 (as well as claim 57 dependent therefrom) is neither anticipated by nor obvious over Chong.

c. Present Claims 37 and 42

The multilayer printed circuit board according to the present invention (claim 37) has via holes formed immediately over the plated-through holes. Accordingly, the wiring length can be decreased to increase the signal transmission speed (page 69, lines 27 to 28 in the specification).

Further, the multilayer printed circuit board according to the present invention (claims 37 and 42) has via holes which cover through holes of the plated-through holes. The electroless plated film of the via hole connects with the electroless plated film of the plated-through hole (Fig. 36 or Fig. 46). Namely, connection is ensured by a metal film constituting the via hole and a metal film constituting the plated-through hole.

Chong does not teach such a constitution. According to Chong, vias 26 and 29 are formed on the through hole 16, but they do not cover the through hole 16. Further, platings 31 of the vias 26 and 29 connect with the conductive polymer 21 filled in the through hole 16. Accordingly, a metal film constituting the via connects with a conductive polymer constituting the through hole.

A plated film has a lower resistance compared to a conductive polymer. Further, contact resistance between metal and metal is lower than metal and conductive polymer. Therefore, the constitution of the present invention (metal connecting with metal) is preferable to achieve a high signal transmission speed. Moreover, since the adhesion between metal and metal is strong, the connection reliability is improved.

Chong does not teach the constitution of the present invention. Further, Chong is silent about the effects of the present invention. Accordingly, a skilled person would not be motivated by Chong to attain the present invention.

In view of the above, Applicants respectfully submit that claims 37, 42 and claims dependent therefrom are neither anticipated by nor obvious over Chong.

d. Present Claims 41 and 62

An additional feature of claims 41 and 62 is the conductor layer covering the surface of the filler exposed from the plated-through hole. The whole bottom surface of the via hole contacts with the conductor layers (for example, 6026a in Fig. 44) on the plated-through hole. The connection reliability between the via hole and the plated-through hole is thereby improved. Further, the whole bottom surface of the via hole can be utilized for signal transmission. In addition, contact resistance between the plated-through hole and the via hole is lowered. Accordingly, a stable signal transmission can be attained and signal transmission speed can be increased.

Chong does not teach about a conductor layer covering the surface of the filler (conductive polymer 21). In Chong, vias 26 and 29 connect directly with the through hole 16. Chong does not teach the constitution of the present invention. Accordingly, a skilled person would not be motivated by Chong to attain the present invention.

In view of the above, Applicants respectfully submit that present claims 41 and 62 and claims dependent therefrom are neither anticipated by nor obvious over Chong.

In view of the foregoing, the Examiner is respectfully requested to reconsider and withdraw the 102(e) rejection based on Chong.

## IV. Response to § 103(a) Rejection of Claims of 22, 23 and 52 over Grescher and Kosaka

Applicants respectfully traverse the rejection of claims 23 and 52 for at least the following reasons. Claim 22 has been canceled.

a. Grescher and Kosaka

Greschner discloses a method for forming metallic layers on a non-conductive surface. Fig. 1F shows the substrate 1 with the recess 4, the sputtered-on copper layer 6, and the electroless-deposited copper 7.

Kosaka discloses a process of plating a molded article of a resin composition. The process comprises electroless plating step and electroplating step (col. 7, lines 7 to 56).

b. Present Claim 23

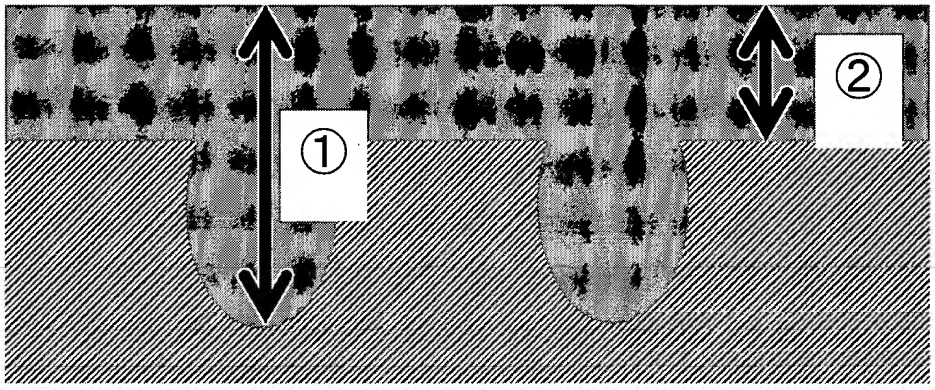
According to the present invention (claim 23), the electroless plated film is complementary to a surface of the roughened surface of the resin insulating substrate board. Thus, the conductor circuit does not have blistering.

Further, the electroless plated film in convex areas of the roughened surface is relatively thicker than the electroless is plated film in concave areas of the roughened surface. In the

etching step, etching solution tends to fail to reach sufficiently to concave areas. Since the electroless plated film in concave areas is thinner, it can be readily and completely stripped off and do not leave unetched residues, so that high inter-conductor insulation dependability is assured even if space between conductor circuits is narrow (see page 38, lines 15 to 20 of the present specification).

While the present invention teaches to form an electroless plated film on the roughened surface, Greschner teaches to form a sputtered-on copper layer on the substrate. Further, while the present invention teaches that the conductor circuit comprises an electroless plated film and an electroplated film, Greschner teaches to form a sputtered-on copper layer and an electroless-deposited copper layer.

Moreover, the present invention is different from Greschner in terms of the thickness of the electroless plated film. Specifically, the electroless plated film of the present invention is thicker in convex areas and thinner in concave areas of the roughened surface. In contrast, as shown below, the electroless copper layer 7 of Greschner is thinner in convex areas (②) and thicker in concave areas (①). With such a constitution, when the electroless copper layer is etched, the layer in the concave areas (①) cannot be completely etched.




Concerning Kosaka, an electroless plating and an electroplating are performed. However, Kosaka is silent about the thickness of the electroless plated film.

In view of the above, neither Greschner nor Kosaka teaches the constitution and the effects of the present invention. Thus, a skilled person would not be motivated to attain the present invention in view of Greschner or Kosaka. Accordingly, Applicants respectfully submit that claims 23 and 52 are neither anticipated by nor obvious over Greschner in view of Kosaka, and thus the § 103 rejection of claims 23 and 52 should be withdrawn.

## V. Response to § 103(a) Rejection of Claims of 25, 26 and 56 over Grescher and Kosaka further in view of Suzuki

Applicants respectfully traverse the rejection of claims 25, 26 and 56 for at least the following reasons. Claim 25 has been amended to depend from claim 23.

a. Suzuki

Suzuki discloses a circuit board. As shown in Fig. 1D, the circuit board comprises a resin substrate 2 and a copper wiring 3 formed from a copper foil 1. The surface of the copper wiring 3 is roughened, and a copper oxide-reduced layer 4 is formed thereon. Further, an electroless nickel plating layer is deposited on the copper oxide-reduced layer 4 (col. 5, lines 43 to 44).

b. Present Claim 25

According to the present invention (claim 25), the electroless plated film comprises copper and at least one metal species selected from the group consisting of nickel, iron and cobalt. Addition of such a metal species inhibits the uptake of hydrogen into the plated metal and reduces the compressive stress of the plated metal. As a result, the resulting film may have an improved adhesion to the resin insulating layer. Furthermore, the metal species forms an alloy with copper and increases the hardness of the plated metal film (page 39, lines 13 to 19 of the present specification).

While the present invention teaches that the electroless plated film comprises copper and at least one metal species selected from the group consisting of nickel, iron and cobalt, Suzuki does not teach that the copper oxide-reduced layer 4 comprises one of nickel, iron and cobalt. The paragraph in col. 4, lines 5 to 9 of Suzuki, on which the Examiner relies, does not teach this feature, either. Suzuki merely describes that a nickel plating layer is deposited on the copper oxide-reduced layer 4. Further, Suzuki does not teach that addition of the above-mentioned

metal species enhances adhesion and hardness of the plated metal film. Accordingly, a skilled person would find no motivation to form an electroless plated film comprising copper and at least one metal species selected from the group consisting of nickel, iron and cobalt.

In addition, Suzuki is silent about an electroless plated film which is relatively thicker in convex areas of a roughened surface and relatively thinner in concave areas of a roughened surface. As set forth above, claim 23 is neither anticipated by nor obvious over Greschner in view of Kosaka. Suzuki neither rectifies the deficiency of these references nor teaches the feature of claim 25. Accordingly, Applicants respectfully submit that claim 25 and dependent claims 26 and 56 are neither anticipated by nor obvious over the cited references, and thus the § 103(a) rejection of 25, 26 and 56 should be withdrawn.

## VI. Response to § 103(a) Rejection of Claim 54 over Furui in view of Greschner

Applicants respectfully traverse the rejection. As set forth above, claim 24, from which claim 54 depends, is neither anticipated by nor obvious over Furui. Greschner does not rectify the deficiencies of Furui. For example, Greschner is silent about the thickness of an electroless plated film formed on the bottom of via holes, since it does not even teach about a via hole. Accordingly, the Examiner is respectfully requested to reconsider and withdraw the § 103(a) rejection of claim 54.

## VII. Conclusion

In view of the above, reconsideration and allowance of claims 9 to 13, 23 to 26, 32, 37, 38, 40 to 46 and 48 to 63 are now believed to be in order, and such actions are hereby earnestly solicited.

If any points remain in issue which the Examiner feels may be best resolved through a personal or telephone interview, the Examiner is kindly requested to contact the undersigned attorney at the local Washington D.C. telephone number listed below.

The USPTO is directed and authorized to charge all required fees, except for the Issue Fee and the Publication Fee, to Deposit Account No. 19-4880. Please also credit any overpayments to said Deposit Account.

Respectfully submitted,

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Marked-Up Drawing
Sheet 1



Fig. 16